PG DEPARTMENT OF COMPUTER SCIENCE				*CLASS: I M.Sc.* Computer Science				
Sem	**Course Type**	**Course Code**	**Course Title**	**Credits**	**Contact Hours/week**	**CIA**	**Ext**	**Total**
I	Elective - 1	21P1DME1(A)	Advanced Computer Organization and Architecture	4	5	25	75	100

Nature of Course				
Knowledge and skill	✓		Employability oriented	
Skill oriented			Entrepreneurship oriented	

Course Objectives

1. To impart knowledge on functions of computer.
2. To learn the working principle of CPU with pipelining.
3. To understand memory concepts, arithmetic operations and the importance of I/O system.
4. To know the importance of parallel computing models and properties of networks.
5. To understand the performance of multi core processors.

Unit	Content	Hrs	K-Level	CLO
I	**Basic Structure of Computers:** Basic operational concepts – Bus structures – Software. **Machine Instructions and Programs:** Memory operations - Instructions and instruction sequencing– Addressing modes – Basic Input / Output operations – Stacks and Queues – Subroutines.	15	Up to K2	1
II	**Basic Processing Unit & Pipelining:** Fundamental concepts – Execution of a complete instruction – Multiple bus organization – Hardwired control – Micro programmed control. **Pipelining:** Basic concepts – Data hazards – Instruction hazards – Influence on instruction sets	15	Up to K3	2
III	**Memory System & Arithmetic:** Basic concepts – Semiconductor RAM – Cache memories - Virtual memory. **Arithmetic:** Addition & Subtraction of signed numbers – Multiplication of positive numbers – Signed operand multiplication. **I/O Organization:** Accessing I/O devices –Interrupts – Direct Memory Access.	15	Up to K4	3
IV	**Parallel Computer Models:** The state of computing - Multiprocessors and multicomputers – Multivector and SIMD computers. **Program and Network properties:** Conditions of parallelism – Program Partitioning and scheduling – Program flow mechanism - system interconnect architectures.	15	Up to K3	4
V	**Multiprocessors and Multicomputers:** Multiprocessor System interconnects – Message Passing Mechanisms. **Multivector and SIMD Computers:** Vector processing principles – SIMD Computer Organizations – **Scalable, Multithreaded, and Dataflow Architectures:** Principles of Multithreading, Fine-Grain Multicomputers. **Software for Parallel Programming:** Parallel Programming Models – Parallel Languages and Compilers – Dependence Analysis of Data Arrays.	15	Up to K4	5

Books for Study

1. "Computer Organization" by Carl Hamacher, ZvonkoVranesic and SafwatZaky, Fifth Edition, Tata McGraw Hill, 2002.
2. "Advanced Computer Architecture – Parallelism, Scalability and Programmability" by Kai Hwang, Naresh Jotwani, , second edition, TMH, New Delhi.

Chapters

Text Book – 1:

Unit I - 1.3, 1.4, 1.5, 2.3, 2.4, 2.5, 2.7, 2.8, 2.9

Unit II - 7.1 - 7.5, 8.1 - 8.4

Unit III – 5.1, 5.2, 5.5, 5.7, 6.1, 6.3, 6.4, 4.1, 4.2, 4.4

Text Book – 2:

Unit IV –- 1.1 – 1.3, 2.1 – 2.4

Unit V – 7.1, 7.4, 8.1, 8.4, 9.2, 9.3, 10.1 – 10.3

Books for Reference

1. "Computer Architecture – A Quantitative Approach" by David A. Patterson and John L. Hennessy, Sixth Edition, Margon Kaufmann Publishers, Elsevier.
2. "Computer Organization and Architecture – Designing for Performance" by William Stallings, Sixth Edition, Pearson Education, 2003.
3. "Computer Architecture and Organization" by John P. Hayes, Third Edition, TataMcGraw Hill, 1998.

Web Resources

1. http://list.zju.edu.cn/kaibu/comparch/
2. https://www.slideshare.net
3. https://cseweb.ucsd.edu/classes/wi14/cse141/pdf/

Rationale for Nature of the course

- Emphasizes the data flow, timing analysis, memory hierarchy, trade off between execution cycles, hardware requirements/cost and software that must be made in order to produce good system design.
- An overview of computer architecture, which stresses the underlying design principles and the impact of these principles on computer performance. General topics include design methodology, processor design, control design, memory organization, system organization, and parallel processing.

Activities on Knowledge and Skill

- Group Discussion
- Quiz
- Seminar

Pedagogy

Chalk and talk Materials, PPT, Assignment, Seminar, Group Discussion and Interaction.

Course Designer(s) Name

1. Mrs. S. Rajalakshmi
2. Mrs. K. R. Ramadevi

Lesson Plan

UNIT	Topics to be Covered	Hours	Mode
I	Basic operational concepts Memory operations Basic Input / Output operations.	4 6 5	Lecture Lecture Lecture & GD
II	Execution of a complete instruction Hardwired control – Micro programmed control Pipelining	5 5 5	Lecture Lecture Lecture & GD
III	Semiconductor RAM – Cache memories Arithmetic Operations Accessing I/O devices –Interrupts, Direct Memory Access	5 5 5	Lecture Lecture, PPT Lecture
IV	The state of computing - Multiprocessors and multicomputers – Multivector and SIMD computers. Conditions of parallelism – Program partitioning and scheduling – Program flow mechanism - system interconnect architectures.	7 8	Lecture Lecture & GD
V	Multiprocessor System interconnects – Message Passing Mechanisms. Vector processing principles – SIMD Computer Organizations - Principles of Multithreading, Fine-Grain Multicomputers. Parallel Programming Models – Parallel Languages and Compilers – Dependence Analysis of Data Arrays.	4 5 6	Lecture Lecture, Assignment Lecture

Course Learning Outcomes

On the completion of the course, the students will be able to

CLOs	COURSE LEARNING OUTCOMES	K - Level
CLO 1	Explain basic operational concepts and identify the use of various Addressing Modes.	Up to K2
CLO 2	Classify types of controls used in instruction execution and inspect the principle of Pipelining.	Up to K3
CLO 3	Compare various memory organizations and focus on Arithmetic Operations and Interrupt techniques to access I/O devices.	Up to K4
CLO 4	Utilize different types of parallelism and interconnect architectures	Up to K3
CLO 5	Assess the use of vector processing, multithreading and parallel processing software.	Up to K4

Mapping of CLOs with POs

CLOs / POs	PO1	PO2	PO3	PO4	PO5	PO6
CLO 1	2	1	-	-	1	-
CLO 2	2	2	2	1	2	-
CLO 3	2	3	2	2	3	2
CLO 4	2	1	-	1	2	-
CLO 5	2	2	1	1	2	2

(3– Advanced Application, 2 – Intermediate Level, 1- Basic Level)

Continuous Internal Assessment (CIA): 25 Marks

Components	Marks	K Level
Test (Average of two tests) (Conducted for 40 marks and converted into 10 marks)	10	(Refer Next Table)
Assignment	5	K4
Seminar	5	K4
Quiz	5	K4
Total	25	

Learning Outcome Based Education & Assessment (LOBE)
Formative - Blue Print – Model for Advanced Computer Organization
Articulation Mapping – K Levels with Courses Learning Outcomes (CLOs)

Internal	CLOs	K- Level	Section A		Section B (Either/or Choice)	Section C (Open Choice)
			Short Answers			
			No. of Questions	K- Level		
CIA I	CLO 1	Up to K2	2	K1	2(K1&K1)	2(K2)
	CLO 2	Up to K3	3	K2	2(K3&K3)	1(K3)
CIA II	CLO 3	Up to K4	2	K2	2(K4&K4)	2(K4)
	CLO 4	Up to K3	3	K1	2(K2&K2)	1(K3)
Question Pattern (CIA I & II)	No. of Questions to be asked		5		4	3
	No. of Questions to be answered		5		2	2
	Marks for each question		2		5	10
	Total Marks for each section		**10**		**10**	**20**

- *CLO5 will be allotted for individual Assignment which carries five marks as part of CIA component.*

Distribution of Section-wise Marks with K Levels *

K Levels	Section A (No Choice)	Section B (Either/or)	Section C (Open Choice)	**Total Marks**	% of Marks without choice	Consolidated %
K1	4	10	-	**14**	23.33	**66**
K2	6	-	20	**26**	43.33	
K3	-	10	10	**20**	33.33	**34**
K4	-	-	-	**-**	-	**-**
Total Marks	**10**	**20**	**30**	**60**	**100**	**100**
K Levels	Section A (No Choice)	Section B (Either/or)	Section C (Open Choice)	**Total Marks**	% of Marks without choice	Consolidated
K1	6	-	-	**6**	10	**33**
K2	4	10	-	**14**	23.33	
K3	-	-	10	**10**	16.67	**17**
K4	-	10	20	**20**	50	**50**
Total Marks	**10**	**20**	**30**	**60**	**100**	**100**

Learning Outcome Based Education & Assessment (LOBE)
Blue Print – Model for Advanced Computer Organization
Articulation Mapping – K Levels with Courses Learning Outcomes (CLOs)

Units	**CLOs**	**K- Level**	**Section A**		**Section B**		**Section C (Either/or Choice)**	**Section D (Open Choice)**
			MCQs		**Short Answers**			
			No of Questions	**K - Level**	**No of Questions**	**K - Level**		
1	CLO 1	Up to K2	2	K1 &	1	K1	2(K1&K1)	1(K2)
2	CLO 2	Up to K3	2	K2 &	1	K2	2(K3&K3)	1(K3)
3	CLO 3	Up to K4	2	K3 &	1	K2	2(K4&K4)	1(K4)
4	CLO 4	Up to K3	2	K2 &	1	K1	2(K2&K2)	1(K3)
5	CLO 5	Up to K4	2	K3 &	1	K3	2(K4&K4)	1(K4)
No. of Questions to be asked			10		5		10	5
No. of Questions to be answered			10		5		5	3
Marks for each question			1		2		5	10
Total Marks for each section			10		10		25	30

- K1 – Remembering and recalling facts with specific answers
- K2 – Basic understanding of facts and stating main ideas with general answers
- K3 – Application oriented – Solving Problems
- K4 – Examining, analyzing, presentation and make inferences with evidences

Distribution of Section – wise Marks with K Levels

K Levels	**Section A (No Choice)**	**Section B (No choice)**	**Section C (Either/or)**	**Section D (Open choice)**	**Total Marks**	**% of Marks without choice**	**Consolidated**
K1	2	4	10	-	**16**	13.33	**13%**
K2	2	4	10	10	**26**	21.67	**22%**
K3	4	2	10	20	**36**	30.00	**30%**
K4	2	-	20	20	**42**	35%	**35%**
Total Marks	10	10	50	50	**120**	100	**100%**